PowerBrake Introduction

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Agenda

- Performance Throttling
- Top-Level Core Clock Gating

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- Control Performance Throttling method
- Top-Level Core Clock Gating

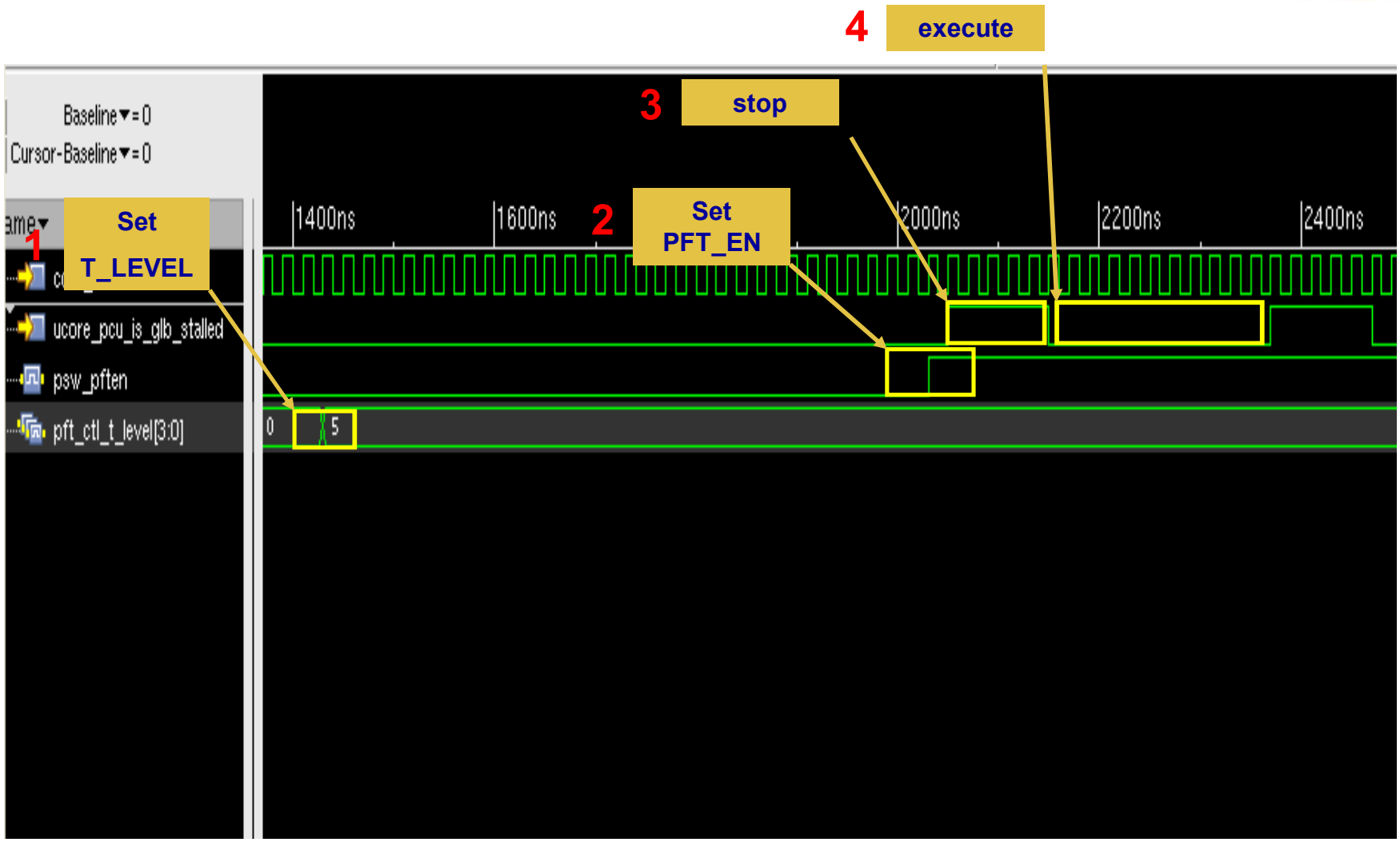
Control Performance Throttling method

- **Performance Throttling**
  - Reduces the power consumption of processor core by throttling processor performance. (setting by PSW ,PFT_EN and PFT_CTL , T_LEVEL)
- **Configurable option in nds-softcore-config**

PowerBrake Configuration	
Performance Throttling	◆ yes ◇ no
Top-Level Core Clock Gating	◇ yes ◆ no

- **System register ir0 and pfr4**

Performance Throttling Diagram



Agenda

- Control Performance Throttling method
- **Top-Level Core Clock Gating**

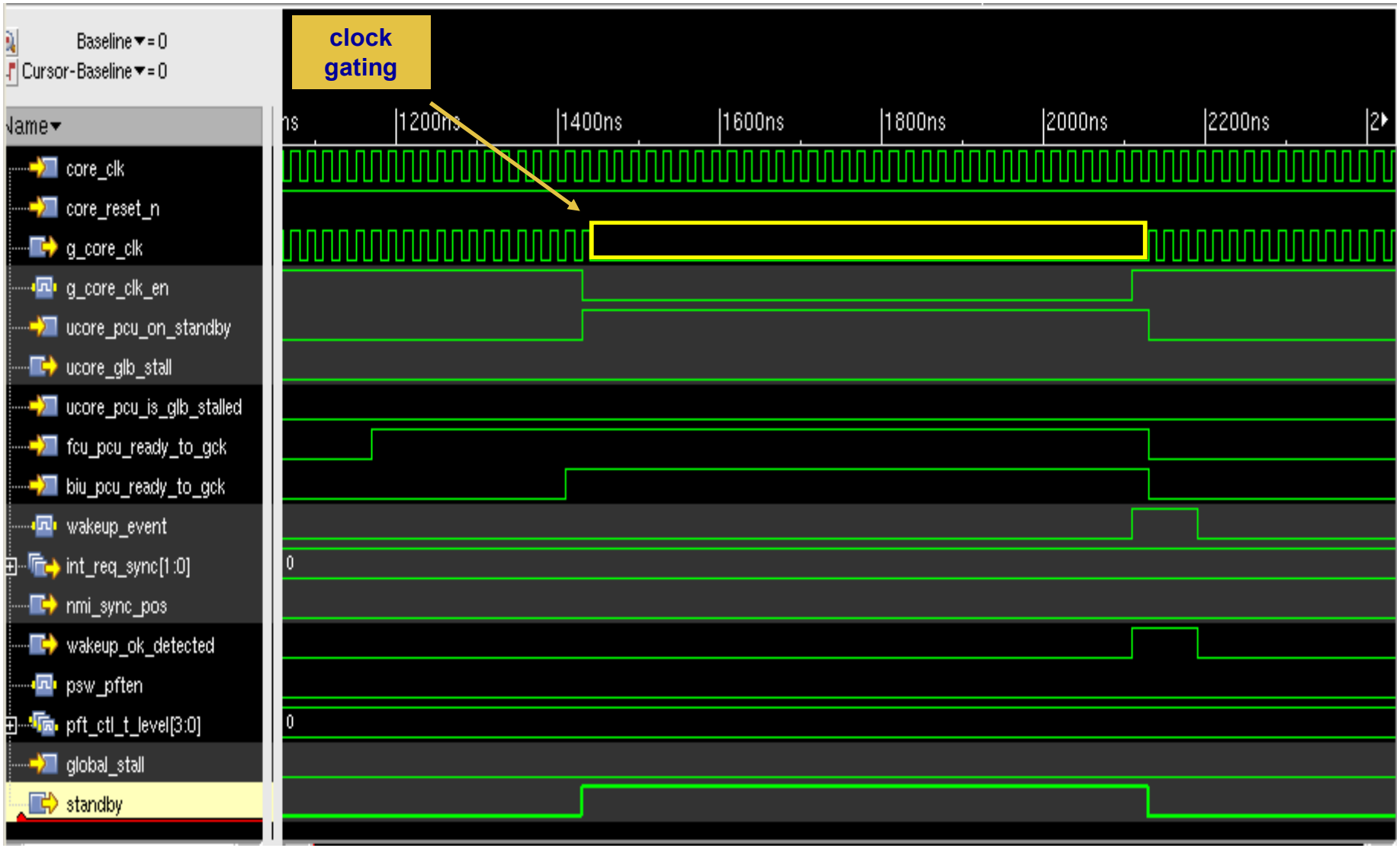
Top-Level Core Clock Gating

- Top-Level Core Clock
  - Reduces the power consumption when the processor core is on standby by gating off the top level core clock.
- Configurable option in nds-softcore-config

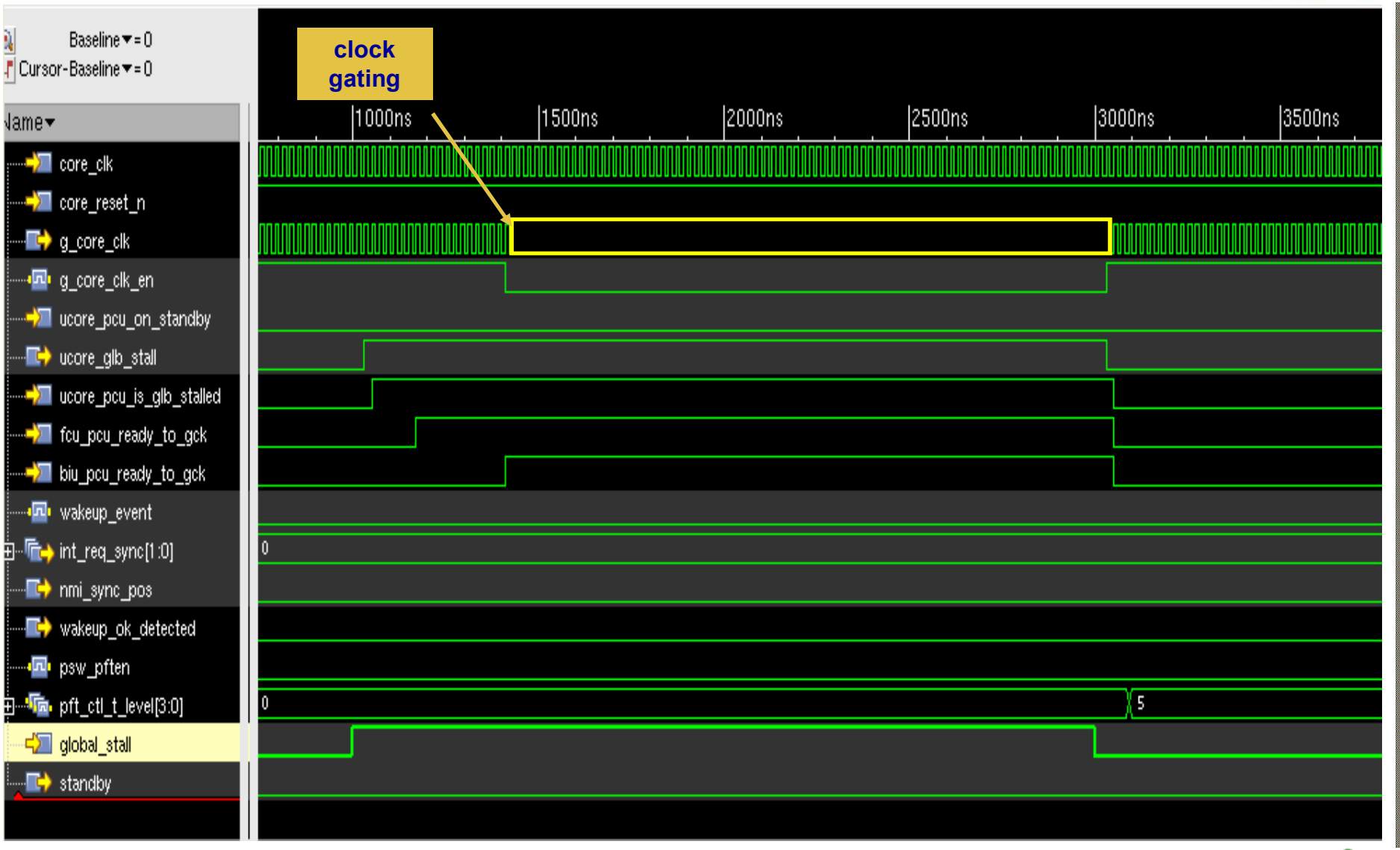
PowerBrake Configuration	
Performance Throttling	◇ yes ◆ no
Top-Level Core Clock Gating	◆ yes ◇ no

- Enter the Top-Level clock gating conditions
  - Standby mode
  - Global stall mode
  - Performance Throttling mode

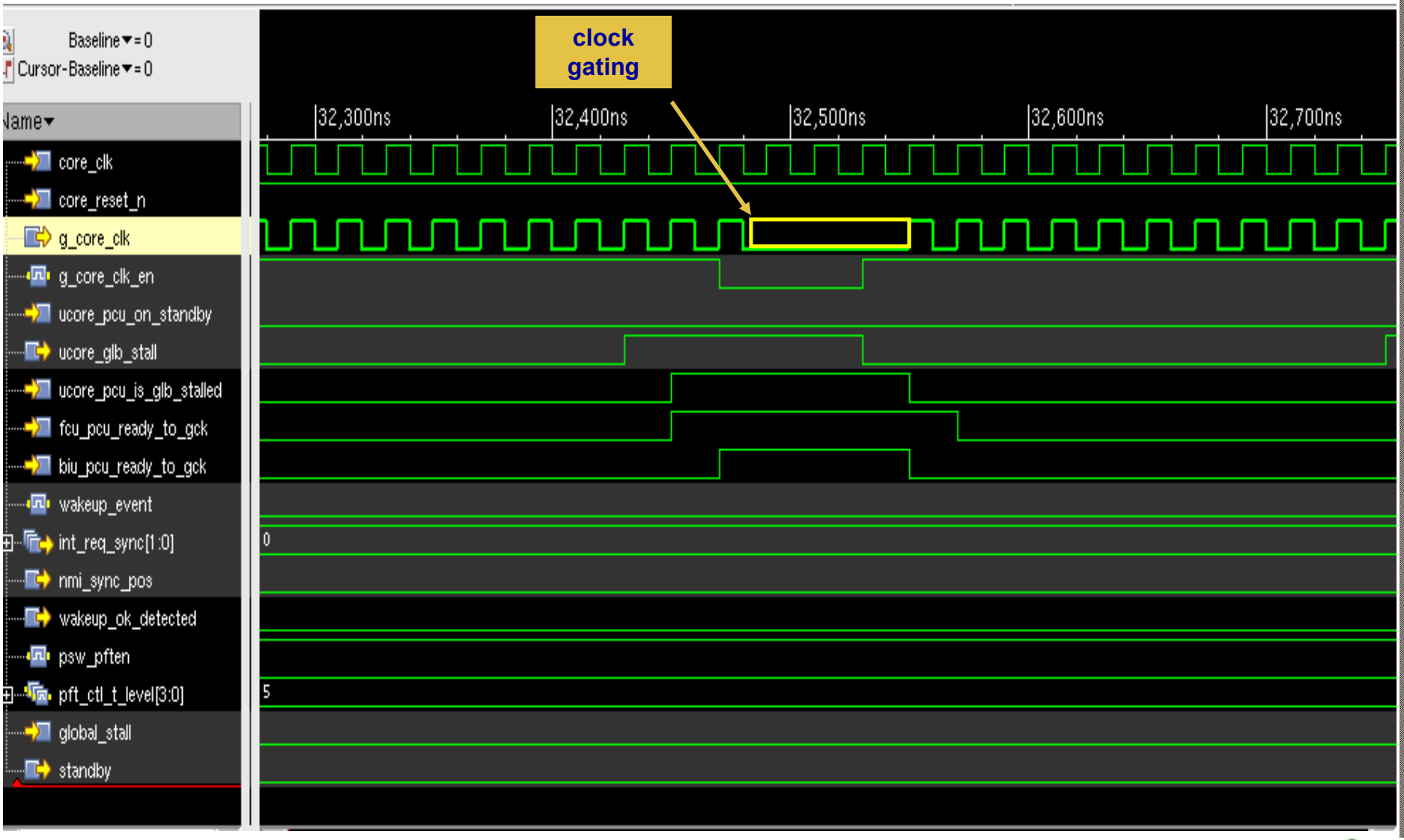
Top-Level core clock gating by standby



Top-Level core clock gating by global stall



Top-Level core clock gating by throttling



Thank You!

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